Printed Pages : 3 EC – 605

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 3042 Roll No.

B. Tech.

(SEM. VI) EXAMINATION. 2006-07

VLSI-TECHNOLOGY

Time : 2 Hours] *[Total Marks : 50*

Note : Attempt all questions.

1 Attempt any **four** of the following : **2.5×4=10**

(a) By means of a sketch, identify the GaAs atoms and their positions and compute the atom density for the principal planes of GaAs in terms of the cube edge and the bond density for these planes.

(b) Gold is introduced into n-type silicon. Show that it will behave as p-type. Repeat for p-silicon; Here, show that the gold will behave as n-type. In both cases, assume that the gold concentration is well below the background concentration.

(c) Describe various factors which must be taken into account in order to grow single crystals which are relatively free from defects in brief.

(d) Describe a Cz furnace. What are its advantages?

(e) Draw the equivalent circuit of a base diffused resistor showing all parasitic elements and explain in brief.

2 Attempt any **four** of the following : **2.5×4=10**

(a) What is the cosmetic inspection and perfection evaluation in wafers?

(b) Does the thickness of the epitaxial wafer pose a problem in epitaxial processing from a stress view point? Discuss your answer.

(c) What are plasma deposition reactors? Why and how are these used?

(d) Discuss the salient properties of Silicon Dioxide in brief.

(e) Considering some premier impurities, describe the respective effects of impurities and damage on the oxidation rate both for Wet Oxidation and Dry Oxidation.

3 Attempt any **two** of the following : **5×2=10**

(a) Differentiate between TTL and ECL with reference to fabrication techniques.

(b) What do you understand by "Device Simulation"? Discuss in brief.

(c) Describe Ion Beam lithography in brief.

4 Attempt any **two** of the following : **5×2=10**

(a) Discuss and describe the basic design rules for miniaturizing VLSI circuit in brief.

(b) With the help of IC process flow diagram, describe briefly, the basic considerations for IC processing for an n-channel, polysilicon MOS.

(c) Discuss various CMOS structures and describe p tub, n tub and twin tub.

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5 Write short notes on any **two** of the following : 5×2=10

(a) IC fabrication techniques for multi-emitter and multi-collector transistors.

(b) MOSIC fabrication technique.

(c) CVD process.