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Printed Pages—3 EC—302

B. TECH

THIRD SEMESTER EXAMINATION, 2002-2003

SWITCHING THEORY & LOGIC DESIGN

2 Hours *Total Marks*

(1) Answer **ALL** the questions.

(2) Make and state assumptions, if required.

Answer any ONE of the following :— (10×1)

(a) (*i*) Using Tabular method and algebraic solution of P.I. Table, obtain minimal realisation of a function shown below :—

$$f(A,B,C,D)=\sum(1,2,3,9,12,13,14)+\sum_{\phi}(0,7,10)$$

(*ii*) What are prime implicants and explain their role in Boolean function representation in its minimal form.

(b) Design a BCD to 7-segment decoder. Assume positive logic. Minimise the functions.

Answer any FOUR of the following :— (3·5×4 = 14)

(a) Convert the decimal integers +21 and −21 into 10's complement and 9's complement.

(b) Convert the above two numbers in binary and express them in six bit (total) signed magnitude and 2's complement.

(c) How is 2's complement advantageous for adder circuit design ? Explain.

(d) Give the truth table for a full-adder and express it as function. Show how 8-full adders may be used to form a 8-bit parallel adder.

(e) Demultiplexer is decoder circuit with an additional enabling input. Do you agree with the above statement ? Justify your answer.

(f) A function is realised as :

$$F(a,b,c) = b'c' + a'c + ab.$$

Redesign the circuit after removing the hazards.

3. Answer any TWO of the following :— (6·5×2 13)

(a) In a synchronous digital circuit, there is only one input. The output goes high whenever an input sequence ...0011101... is detected.

(i) Draw the state transition diagram for the above circuit.

(ii) How many states does the circuit have ?

(iii) How many flip-flops does the circuit need ?

(iv) Design the circuit using D-FFs.

(b) (i) A sequential digital circuit has at least one feedback path, whereas a combinational circuit has none. Do you agree with the above statement ? Explain.

(ii) How do undesired states occur in synchronous sequential digital circuits ? How can one prevent entry into an undesired state ?

(iii) Distinguish between synchronous and asynchronous digital sequential circuits. Explain, using example circuits of three bit binary counters of both the types.

(c) (i) Is the master-slave option limited to J-K flip-flops only ? Explain.

(*ii*) Using a T-FF, design a R-S FF.

(*iii*) Using any type of flip-flops, design a 4-bit synchronous counter that up-counts in gray-code.

4. Answer any TWO of the following :— (6·5×2=13)

(*a*) A hypothetical 32-bit floating point number system has base = 8 and radix = 2. It has 22-bit 2's complement normalised mantissa and 10 bit excess – 512 exponent. Zero is represented by a sequence of 32 zeroes. Find (*i*) Number of unused codes, (*ii*) Range of number system and (*iii*) Finest resolution.

(*b*) (*i*) How does parity help in error-detection ?

(*ii*) Can a wrongly received sequence be still detected as correct, despite using parity ? If no, explain. If yes, justify the use of parity.

(*iii*) What are critical race and non-critical race ? Is race-around condition an example of race ? Justify.

(*c*) Suppose circuit of Fig. 1 is operating in fundamental mode. Analyse the circuit by forming the (*i*) Flow Table, (*ii*) Transition flow diagram and (*iii*) Transition diagram, if it exists.

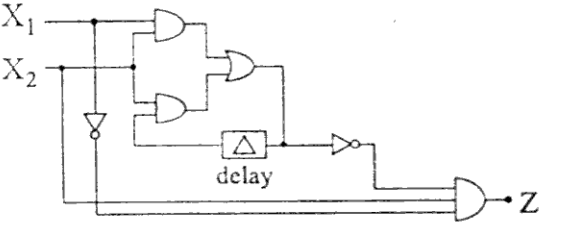

Fig. 1