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EC–605

B. TECH.

SIXTH SEMESTER EXAMINATION, 2003-2004

VLSI–TECHNOLOGY

Time : 2 Hours *Total Marks : 50*

Note : Attempt **ALL** the questions.

1. Attempt any *FOUR* of the following :— **(3×4)**

(a) In bipolar IC, the transistors are suitably connected to act as diode. How many ways are there to connect the transistor to form a monolithic diode ? Which diode do you rate as optical ? Justify your answer.

(b) Describe a lateral p-n–p transistor. Why is its current gain low ?

(c) Draw the equivalent circuit of a base diffused resistor, showing all parasitic elements. What can externally be done to minimize the effect of parasitic elements ?

(d) What are the techniques to form oxide layer ? What are the applications of silicon dioxide layer ? Describe in brief.

(e) Define Scale of Integration. Differentiate between Scale of Integration and Package Density. What are the advantages of integrated circuit over discrete components ? Explain.

(f) What are various operations performed during wafer preparation ? Explain one machining and one chemical operation required to perform during wafer preparation.

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2. Attempt any *FOUR* parts of the following :— (3×4)

(a) What is Fick's Law of diffusion ? Boron is diffused into an *n*-type single crystal substrate with doping concentration of 10^{15} atoms/cm^3. Assuming diffusion function as Gaussian, if diffusion time is 1 hour, surface concentration is 1×10^{18} cm^{-3} and depth of junction is 2μ m, determine diffusivity.

(b) What do you mean by Ion Implantation ? If an analyzing magnet bends the ion beam through 45° and L = r = 50 cm, find the displacement D that would be seen if B_{10} is sent through the system when it is tuned for B_{11}. If the extraction potential is 2 kV, find field required.

(c) Explain Proximity Printing and Projection Printing and compare these two.

(d) Explain negative photoresists and etchant with examples.

(e) Write short note on Photolithography.

(f) Explain epitaxial growth. What are different techniques of epitaxial layer growth ? Describe any one.

3. Attempt any *TWO* parts of the following :— (6·5×2)

(a) What do you mean by Sputtering ? Explain Sputtering Yield. Draw the schematic diagram of single parallel-plate sputtering system and its working.

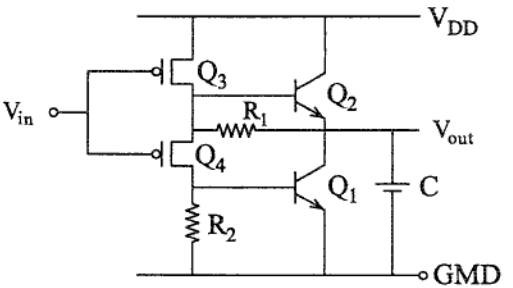
(b) Draw the circuit diagram, of ECL OR/NOR gate and explain its working with the help of transfer characteristic curve. What are the advantages, disadvantages and area of application of ECL logic circuit ?

(c) What do you mean by multiemitter transistor ? Draw layout and structure of multiemitter transistor ? What are its advantages and uses ? Explain.

4. Attempt any *TWO* of the following :— **(6·5×2)**

(a) Compare CMOS and Bipolar technology. What are different steps involved in the fabrication of a *n*-MOS device ? Explain each step with suitable diagrams.

(b) A circuit is shown in the figure —



Name the circuit. Explain its features and role of resistances R_1 and R_2.

(c) What do you mean by Latch Up ? Explain, with the help of mathematical expressions, how latch up can be avoided in CMOS technology.