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(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 0306 Roll No.

B. Tech.

(SEM. VII) EXAMINATION, 2007-08

DIGITAL SYSTEM DESIGN USING VHDL

Time : 3 Hours] *[Total Marks : 100*

Note : *(1) Attempt **all** questions.*

*(2) **All** questions carry **equal** marks.*

(3) Be precise in your answer.

*(4) No **second** answer book will be provided.*

1 Attempt any **four** parts : **5×4=20**

(a) What are the logic levels described in the std_ulogic in IEEE-1164 package? Describe the purpose of each level. What kind of hardware would the symbol 'Z' translate to in a VHDL code? Write the Entity and Architecture for implementing the following function :

f = sum m(1,2,4,6,9)

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(b) A Moore machine with two inputs x and y and one output z, has the following state table :

	NS				
PS	*00*	*01*	*10*	*11*	*Z*
1	1	2	1	3	0
2	1	3	1	2	1
3	2	2	3	1	0

Write VHDL code to describe the state machine at behavioural level. Assume gates with 5 ns delay.

(c) Write VHDL code for a 1-bit full adder using logic equations. Write VHDL code for a 8-bit full adder using the module defined earlier as a component.

(d) What is operator overloading in VHDL? Illustrate with a suitable example. Write VHDL code for a D Flip-flop with asynchronous reset signal, and a clock gate signal EN. Both the signals are active high.

(e) Write VHDL code for a 8-bit Johnson counter.

(f) Write a short note on compilation, simulation and synthesis of VHDL code.

2 Attempt any **four** parts : 5×4=20

(a) Show the block diagram for a 8-bit serial multiplier. Use suitable shift registers, full adders, flip-flops and gates. Draw the state graph for the serial multiplier controller and implement it in hardware.

(b) Write VHDL code for a 16-bit serial multiplier.

(c) Design a multiplier to multiply two, 8-bit unsigned numbers. The result is a 16-bit product. Use any method of your choice. Show the datapath and control path of the solution explicitly.

(d) Construct an ASM chart for the following state table. Each decision box can only test one variable. Write VHDL code for the state machine based on the ASM chart.

N.S. Outputs

PS	X_1X_2 : *00*	*01*	*10*	*11*
S0	S3,00	S2,10	S1,11	S0,01
S1	S0,10	S1,10	S2,01	S3,00
S2	S3,11	S0,11	S1,01	S1,11
S3	S2,00	S2,00	S1,10	S0,00

(e) Draw block diagram for a divider that divides an 8-bit dividend with a 4-bit divisor and a suitable quotient. The dividend register is loaded with a signal start = 1. Construct an ASM chart for the control circuit.

(f) Realize the ASM chart in part *d* using microprogram control. What will be the contents of the microprogram memory? Draw a block diagram of your implementation using ROM, multiplexers, flip-flops etc.

3 Attempt any **four** parts : 5×4=20

(a) Explain the purpose and working of programmable interconnects used in Xilinx FPGAs.

(b) What is the advantage of one-hot state assignment method over other methods? Where is it preferred? Design a '1001' sequence detector using one-hot assignment. Use JK-flip flops.

(c) Add two floating point numbers, with 5-bit fraction and 5-bits exponent. F1 = 1.0011, E1 = 11011, F2 = 0.1110, E2=10101. Also draw a flow chart for a floating point multiplier.

(d) Draw an ASM chart for a fixed point multiplier. Define the control signals used.

(e) Write a short note on Xilinx 3000 series FPGAs.

(f) Implement an 8-bit binary counter using 3000 series logic cell. The counter has an asynchronous reset signal.

4 Attempt any **four** parts : **5×4=20**

(a) With the help of a block diagram, write a short note on 6116 Static RAM.

(b) Write VHDL code for a simple memory model with 512 bytes of memory arranged in 8-bits of data at each location.

(c) Write VHDL code for a simplified 486 memory bus interface unit.

(d) For a static CMOS RAM device, explain the read cycle timing diagram, WE* controlled write cycle timing diagram and CS* controlled write cycle timing diagram.

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(e) How would you test a Memory device? Write VHDL code for a tester for a simple memory model.

(f) Write VHDL code for testing the RAM timing model.

5 Attempt any **four** parts : 5×4=20

(a) What is the standard serial data format? Explain all the terms. What is the typical ratio of the bit rate and bit clock frequency in a UART? How can the faster bit clock frequency improve noise immunity of a UART receiver?

(b) Explain the operation of a UART with the help of a detailed block diagram.

(c) Write VHDL code to model an ALU for a microprocessor to perform the following operations : AND, OR, EXOR, Complement, add, add with carry. Assume 8-bit datapath.

(d) Illustrate the operation of UART transmitter controller with a suitable SM chart. Write VHDL code for the controller.

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(e) Illustrate the operation of a 68HC05 microcontroller with a top level VHDL code.

(f) Write a short note on the 6805 instruction set.
