

# M.C.A. <br> (SEM. II) THEORY EXAMINATION 2010-11 <br> <br> COMPUTER ARCHITECTURE AND <br> <br> COMPUTER ARCHITECTURE AND MICROPROCESSOR 

 MICROPROCESSOR}

Time : 3 Hours
Total Marks : 100
Note:- (1) Attempt ALL questions. All questions carry equal marks.
(2) Assume suitable missing data and specify it clearly.

1. Attempt any two parts of the following: $\quad(10 \times 2=20)$
(a) Describe parallel computing. Why do we need parallel computers? Give one analogy to explain your answer.
(b) Explain the Feng's classification of computer architectures in detail.
(c) (i) Machine A has a clock cycle time of 2 ns and a CPI of 4.0 for a program and Machine $B$ has a clock cycle time of 2 ns and a CPI of 1.2 for the same program. Which machine is faster and by how much ?
(ii) Explain the role of data flow graphs in parallel computing.
2. Attempt any two parts of the following : ( $10 \times 2=20$ )
(a) Compare the advantages and disadvantages of the S -access and C -access memory organizatwons for pipelined vector accessing.
(b) Consider the following piftefifledwubbekstorn wine.cem stages. All successor stages after each stage must be used in successive clock periods.

(i) Write out the reservation table for this pipeline with six columns and four rows.
(ii) Show the initial collision vector.
(iii) Draw the state diagram which shows all possible latency cycles.
(iv) What is the value of the minimal ayerage latency (MAL)?
(c) (i) Implement the dot-product operation with internal data forwarding between a multiply unit and an add unit.
(ii) Write notes on SMD array processors.
3. Attempt any two paris of the following :
( $10 \times 2=20$ )
(a) Compare the Butteffly networks, hypercube networks and shuffle exchange network in terms of switches elements, diameters, Bisection widths and edges/nodes.
(b) Give parallel algorithm of $\mathrm{O}\left(\mathrm{n} \log _{2} \mathrm{n}\right)$ for matrix multiplication. Show the allocation of the elements of two $4 \times 4$ matrices in a 4 -cube of 16 PES.
(c) Construct a 64 -input omega network using $4 \times 4$ switch modules in multiple stages. How many permutations can be implemented directly in a single pass through the network without blocking?
4. Attempt any two parts of the following :
(a) Explain various multiprocessor scheduling strategies.
(b) Draw data flow graphs to represent the following computations :
(i) if $(a=b)$ and $(c<d)$
then $c \leftarrow c-a$
else $\mathrm{c} \leftarrow \mathrm{c}+\mathrm{a}$
(ii) For $\mathrm{i} \leftarrow 1$ to m do

$$
\begin{aligned}
& c[i] \leftarrow 0 \\
& \text { for } j \leftarrow 1 \text { to } n \text { do } \\
& \quad c[i] \leftarrow c[i]+a[i, h] * b[j]-
\end{aligned}
$$

(c) Discuss the register set of intel 16 bit microprocessor.
5. Attempt any four parts of the following :
$(5 \times 4=20)$
(a) Explain the difference among the machine language, assembly language and high level language.
(b) Explain the functions of ALE and $1 O / \bar{M}$ signals of the 8085 microprocessors.
(c) Write a assembly language program of 8085 to performs the following :
(i) Load the number 8 BH in register D .
(ii) Load the number 6 FH in register C .
(iii) Increment the contents of register C by one.
(iv) Add the contents of registers C and D and display the sum at the outport PORT1.
(d) What are the control signals necessary in memory-mapped I/O ? Explain.
(e) Explain the functions of the following routine :

## LXI SP, STACK

PUSH B
PUSH D
POP B
POP D
RET
(f) What is the advantage of using assembly language instead of writing a program directly in machine language ?

